CLAIMS

1. A fabrication method for forming pores within a central area of a semi-conductive or conductive surface, comprising the steps of:

forming a semi-conductive or conductive surface on a substrate in a manner ensuring that upon application of an electric field at the semi-conductive or conductive surface an intensity of the electric field at a central area of the surface is at least as great as an intensity of the electric field at a perimeter of the surface; and

anodizing the semi-conductive or conductive surface by generating the electric field at the semi-conductive or conductive surface to form a porous region within the semi-conductive or conductive surface.

2. A method according to claim 1 wherein the forming step further comprises:

forming a dielectric layer on the substrate;

removing a portion of the dielectric layer, leaving a remaining part of the dielectric layer and exposing a central region of the substrate; and

forming the semi-conductive or conductive surface on a portion of the remaining part of the dielectric layer and on the central region of the substrate.

3. A method according to claim 2 further comprising the step of anodizing the semi-conductive or conductive surface to form an anodized region in the semi-conductive or conductive surface above an area of contact between the semi-conductive or conductive surface and the substrate.

4. A method according to claim 3, further comprising:

forming a conductive layer on the semi-conductive or conductive surface;

forming a second conductive layer on the first conductive layer;

forming a second dielectric layer on the second conductive layer;

forming a third conductive layer on the second dielectric layer; and

removing a portion of the second conductive layer, the second dielectric layer and the third conductive layer above the anodized region.

5. A method according to claim 2, further comprising:

forming a conductive layer on the semi-conductive or conductive surface;

forming a second dielectric layer on the conductive layer;

forming a second conductive layer on the second dielectric layer; and

removing a portion of the first conductive layer, the second dielectric layer and the second conductive layer above an area of contact between the semi-conductive or conductive surface and the substrate, leaving a remaining part of the second conductive layer and exposing a central region of the semi-conductive or conductive surface.

6. A method according to claim 5, further comprising:

anodizing the central region of the semi-conductive or conductive surface to form an anodized region in the semi-conductive or conductive surface; and

forming a third conductive layer on the remaining part of the second conductive layer and on the anodized region.

7. A method according to claim 1 wherein the forming step further comprises:

forming the semi-conductive or conductive surface on the substrate;

forming a conductive shield on the semi-conductive or conductive surface; and

removing a portion of the conductive shield, exposing a central region of the semi-conductive or conductive surface and leaving a remaining part of the conductive shield.

8. A method according to claim 7 further comprising the step of anodizing the central region of the semi-conductive or conductive surface to create an anodized region in the semi-conductive or conductive surface.

9. A method according to claim 8, further comprising:

removing the remaining part of the conductive shield;

forming a dielectric layer on the semi-conductive or conductive surface; and

removing a portion of the dielectric layer above the anodized region.

10. A method according to claim 9, further comprising:

forming a conductive layer on the remaining portion of the first dielectric layer and on the anodized region;

forming a second dielectric layer on the conductive layer;

forming a second conductive layer on the second dielectric layer; and

removing a portion of the third conductive layer and the second dielectric layer above the anodized region.

11. A method according to claim 1, further comprising the step of selecting silicon as the semi-conductive or conductive surface.

12. A method according to claim 7, further comprising the step of selecting a metal as the conductive shield.

13. A fabrication method for improving electron emission in a selected area of a semi-conductive or conductive flat emitter surface, comprising:

forming a semi-conductive or conductive flat emitter surface on a substrate in a manner ensuring that upon application of an electric field at the semi-conductive or conductive flat emitter surface an intensity of the electric field at a central area of the flat emitter surface is at least as great as an intensity of the electric field at a perimeter of the flat emitter surface; and

anodizing the semi-conductive or conductive flat emitter surface by generating the electric field at the semi-conductive or conductive flat emitter surface to form pores in the semi-conductive or conductive flat emitter surface wherein the pores are proportionally concentrated according to the electric field intensity.

14. A method for improving electron emission according to claim 13 wherein the forming step further comprises:

forming a dielectric layer on the substrate;

removing a portion of the dielectric layer, leaving a remaining part of the dielectric layer and exposing a central region of the substrate; and

forming the semi-conductive or conductive flat emitter surface on a portion of the remaining part of the dielectric layer and on the central region of the substrate.

15. A method for improving electron emission according to claim 14 further comprising the step of anodizing the semi-conductive or conductive surface to form an anodized region of the semi-conductive or conductive surface above the central region of the substrate.

16. A method for improving electron emission according to claim 15, further comprising:

forming a second dielectric layer on the semi-conductive or conductive flat emitter surface;

forming a conductive layer on the second dielectric layer;

forming a second conductive layer on the first conductive layer;

forming a third dielectric layer on the second conductive layer;

forming a third conductive layer on the third dielectric layer; and

removing a portion of the second conductive layer, the third dielectric layer and the third conductive layer above the anodized region.

17. A method for improving electron emission according to claim 14, further comprising:

forming a conductive layer on the semi-conductive or conductive flat emitter surface;

forming a second dielectric layer on the conductive layer;

forming a second conductive layer on the second dielectric layer; and

removing a portion of the first conductive layer, the second dielectric layer and the second conductive layer above an area of contact between the semi-conductive or conductive flat emitter surface and the substrate, leaving a remaining part of the second conductive layer and uncovering a central region of the semi-conductive or conductive flat emitter surface.

18. A method for improving electron emission according to claim 17, further comprising:

anodizing the central region of the semi-conductive or conductive flat emitter surface to form an anodized region in the semi-conductive or conductive surface;

forming a third dielectric layer on the anodized region; and

forming a third conductive layer on the remaining part of the second conductive layer and on the third dielectric layer.

19. A method for improving electron emission according to claim 13 wherein the forming step further comprises:

forming the semi-conductive or conductive flat emitter surface on the substrate;

forming a conductive shield on the semi-conductive or conductive flat emitter surface;

removing a portion of the conductive shield to expose a central region of the semi-conductive or conductive flat emitter surface.

20. A method for improving electron emission according to claim 19 further comprising the step of anodizing the central region of the semi-conductive or conductive flat emitter surface after removing a portion of the conductive shield.

21. A method for improving electron emission according to claim 20, further comprising:

removing the remaining portion of the conductive shield;

forming a dielectric layer on the semi-conductive or conductive flat emitter surface; and

removing a portion of the dielectric layer above the central region of the semi-conductive or conductive flat emitter surface.

22. A method for improving electron emission according to claim 21, further comprising:

forming a second dielectric layer on the anodized region;

forming a conductive layer on the remaining portion of the first dielectric layer and on the second dielectric layer;

forming a third dielectric layer on the conductive layer;

forming a second conductive layer on the third dielectric layer; and

removing a portion of the third conductive layer and the third dielectric layer above the anodized region.

23. A method according to claim 13, further comprising the step of selecting silicon as the semi-conductive or conductive surface.

24. A method according to claim 19, further comprising the step of selecting a metal as the conductive shield.

25. A method for fabricating a porous electron emission device to improve electron emission characteristics of the porous electron emission device, the method comprising:

forming a dielectric barrier over a substrate;

opening at least one selected region of the dielectric barrier to expose a central region of the underlying substrate where flat emitters are to be located;

forming a semi-conductive or conductive surface over the dielectric barrier and the central region of the underlying substrate; and

anodizing the semi-conductive or conductive surface wherein a central area of the semi-conductive or conductive surface has improved electron emission efficiency over an outer perimeter thereof.

26. A method for fabricating porous semi-conductive or conductive flat emitters utilized as field emission emitters to improve their electron emission characteristics, the method comprising:

forming a semi-conductive or conductive surface over a substrate;

forming a metal shield over the semi-conductive or conductive surface;

opening a selected region of the metal shield to expose a central region of the semi-conductive or conductive surface where the flat emitter is to be located; and

anodizing the semi-conductive or conductive surface to form a porous region in the central region of the semi-conductive or conductive surface wherein the metal shield causes an electric field intensity in the semi-conductive or conductive surface to be substantially uniform so that an intensity of the electric field at a central area of the surface is at least as great as an intensity of the electric field at a perimeter of surface.

27. An electron emission device comprising:

a dielectric barrier positioned on a portion of a substrate and at least partially defining a perimeter of a central region of the substrate;

a semi-conductive or conductive layer positioned on at least a portion of the dielectric barrier and on the central region of the substrate; and

a porous region located in a surface area of the semi-conductive or conductive layer above the central region of the substrate wherein a concentration of pores is not greater in a perimeter than in a central area of the semi-conductive or conductive layer.

a porous region located in a surface area of the semi-conductive or conductive layer above the central region of the substrate wherein a concentration of pores in a central area of the semi-conductive or conductive layer is at least as great as a concentration of pores in a perimeter of the semi-conductive or conductive layer.

28. An electron emission device according to claim 27, further comprising:

a dielectric layer positioned on the semi-conductive or conductive layer;

a first conductive layer positioned on the dielectric layer;

a second conductive layer positioned on at least a portion of the first conductive layer except over the porous region of the semi-conductive or conductive layer;

a second dielectric layer positioned on at least a portion of the second conductive layer; and

a second conductive layer positioned on at least a portion of the second dielectric layer.

29. An electron emission device according to claim 27, further comprising:

a first conductive layer positioned at least a portion of the semi-conductive or conductive layer except over the porous region of the semi-conductive or conductive layer;

a dielectric layer positioned on at least a portion of the first conductive layer;

a second conductive layer positioned on at least a portion of the dielectric layer;

a second dielectric layer positioned on the porous region of the semi-conductive or conductive layer; and

a third conductive layer positioned on at least a portion of the second conductive layer and on the second dielectric layer.